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In the abstract:

Replace the abstract with the following version.

A3
A method for fabricating a contact hole for a semiconductor memory element. The memory element includes a silicon substrate, an intermediate dielectric layer on the substrate, and an upper layer on the intermediate dielectric layer. The method includes forming a perforated mask on the upper layer, the mask including a material that exhibits temperature stability. The upper layer and a depression are etched into the intermediate dielectric layer as far as a residual thickness using the perforated mask. A layer including $O_3/TEOS-SiO_2$ is deposited onto a structure thus obtained. The layer including $O_3/TEOS-SiO_2$ is removed from a bottom of the depression by etching. The depression is lowered by etching to produce the contact hole as far as an interface with the silicon substrate, the silicon substrate being uncovered, and the layer including $O_3/TEOS-SiO_2$ serving as a lateral seal of the upper layer during the lowering of the depression.